Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application.

Listing of Claims:

1. (Currently Amended) An SRAM-compatible memory including a plurality of memory banks each having a plurality of DRAM cells arranged in a matrix form defined by rows and columns, the DRAM cells interfacing with an external system which does not provide a separate timing period for performing a refresh operation for the DRAM cells, comprising:

the memory banks for receiving and storing input data externally provided, the memory banks generating bank information signals each indicating whether a corresponding memory bank is subjected to an invalid read-access;

a parity generator for receiving the input data to generate input parity, the input parity being determined based on the input data and a preset parity value;

a parity bank for storing the input parity and generating a parity bank information signal indicating whether the parity bank is subjected to the invalid read-access;

a refresher timer generating a refresh request signal periodically to activate the refresh operation for both the memory banks and the parity bank; and

a data corrector receiving the bank information signals and fetched data from the memory banks and generating output data having same value as the input data by correcting data fetched from a memory bank subjected to the invalid read-access if a checked parity value is different from the preset parity value, the checked parity value being obtained using the fetched data provided from the memory banks and parity data fetched from the parity bank,

wherein the data corrector comprises:

a bank data control unit for receiving the bank information signals and the fetched data to provide bank control data, any of the bank control data corresponding to fetched data provided from any of the memory banks subjected to the invalid read-access has a first logic value;

a parity data control unit for receiving the parity information signal and the parity data fetched from the parity bank to provide parity control data;

a discriminating unit for receiving the bank control data and the parity control data and providing discrimination data having a second logic value contrary to the first logical value if the fetched parity data is different from the input parity; and

a selecting unit for selecting the bank control data or the discrimination data in response to the bank information signals to generate the output data,

wherein the refresh operation is independently performed with respect to the respective memory banks, and is prevented from being simultaneously performed with respect to two or more memory banks.

2. (Cancelled)

3. (Currently Amended) The SRAM-compatible memory according to claim 1~~2~~, wherein the parity bank has a substantially same capacity and structure as each of the memory banks.

4. (Currently Amended) The SRAM-compatible memory according to claim 1~~2~~, wherein the memory banks each independently store corresponding one of the input data.

5. (Currently Amended) The SRAM-compatible memory according to claim 1~~2~~, wherein each of the memory banks independently performs a read-access operation in response to a read command externally provided.

6. (Cancelled)

7. (Currently Amended) An SRAM-compatible memory including a plurality of memory banks each having a plurality of DRAM cells arranged in a matrix form defined by rows and columns, the DRAM cells interfacing with an external system which does not provide a separate timing period for performing a refresh operation for the DRAM cells, comprising~~The SRAM-compatible memory according to claim 2, wherein~~:

the memory banks for receiving and storing input data externally provided, the memory

banks generating bank information signals each indicating whether a corresponding memory bank is subjected to an invalid read-access;

a parity generator for receiving the input data to generate input parity, the input parity being determined based on the input data and a preset parity value;

a parity bank for storing the input parity and generating a parity bank information signal indicating whether the parity bank is subjected to the invalid read-access;

a refresher timer generating a refresh request signal periodically to activate the refresh operation for both the memory banks and the parity bank; and

a data corrector receiving the bank information signals and fetched data from the memory banks and generating output data having same value as the input data by correcting data fetched from a memory bank subjected to the invalid read-access if a checked parity value is different from the preset parity value, the checked parity value being obtained using the fetched data provided from the memory banks and parity data fetched from the parity bank,

wherein the data corrector comprises:

a bank data control unit for receiving the bank information signals and the fetched data to provide bank control data, any of the bank control data corresponding to fetched data provided from any of the memory banks subjected to the invalid read-access has a first logic value;

a parity data control unit for receiving the parity information signal and the parity data fetched from the parity bank to provide parity control data;

a discriminating unit for receiving the bank control data and the parity control data and providing discrimination data having a second logic value contrary to the first logical value if the fetched parity data is different from the input parity; and

a selecting unit for selecting the bank control data or the discrimination data in response to the bank information signals to generate the output data,

wherein the bank data control unit includes a plurality of first logic devices each performing logic AND operation with respect to an inverted signal of corresponding one of the bank information signals and the fetched data provided from corresponding one of the memory banks to generate corresponding one of the bank control data; and

the parity data control unit includes a second logic device performing logic AND

operation with respect to an inverted signal of the parity information signal and the parity data to provide the parity control data, and

wherein the refresh operation is independently performed with respect to the respective memory banks, and is prevented from being simultaneously performed with respect to two or more memory banks.

8. (Previously Presented) The SRAM-compatible memory according to claim 7, wherein the parity bank has a substantially same capacity and structure as each of the memory banks.

9. (Original) The SRAM-compatible memory according to claim 7, wherein the memory banks each independently store corresponding one of the input data.

10. (Original) The SRAM-compatible memory according to claim 7, wherein each of the memory banks independently performs a read-access operation in response to a read command externally provided.

11. (Cancelled)

12. (Original) The SRAM-compatible memory according to claim 7, wherein the selecting unit includes a plurality of multiplexers each receiving corresponding one of the bank control data from corresponding one of the first logic devices and the discrimination data from the discriminating unit and selecting the corresponding one of the bank control data or the discrimination data in response to corresponding one of the bank information signals.

13. (Original) The SRAM-compatible memory according to claim 12, wherein the multiplexers each select the discrimination data when the corresponding one of the bank information signals indicates that the fetched data is provided from a memory bank subjected to the invalid read-access.

14. (Original) The SRAM-compatible memory according to claim 13, wherein the multiplexers each select the corresponding one of the bank control data when the corresponding one of the bank information signals indicates that the fetched data is valid.

15. (Currently Amended) ~~The SRAM-compatible memory according to claim 2,~~An SRAM-compatible memory including a plurality of memory banks each having a plurality of DRAM cells arranged in a matrix form defined by rows and columns, the DRAM cells interfacing with an external system which does not provide a separate timing period for performing a refresh operation for the DRAM cells, comprising:

the memory banks for receiving and storing input data externally provided, the memory banks generating bank information signals each indicating whether a corresponding memory bank is subjected to an invalid read-access;

a parity generator for receiving the input data to generate input parity, the input parity being determined based on the input data and a preset parity value;

a parity bank for storing the input parity and generating a parity bank information signal indicating whether the parity bank is subjected to the invalid read-access;

a refresher timer generating a refresh request signal periodically to activate the refresh operation for both the memory banks and the parity bank; and

a data corrector receiving the bank information signals and fetched data from the memory banks and generating output data having same value as the input data by correcting data fetched from a memory bank subjected to the invalid read-access if a checked parity value is different from the preset parity value, the checked parity value being obtained using the fetched data provided from the memory banks and parity data fetched from the parity bank,

wherein the data corrector comprises:

a bank data control unit for receiving the bank information signals and the fetched data to provide bank control data, any of the bank control data corresponding to fetched data provided from any of the memory banks subjected to the invalid read-access has a first logic value;

a parity data control unit for receiving the parity information signal and the parity data fetched from the parity bank to provide parity control data;

a discriminating unit for receiving the bank control data and the parity control data and providing discrimination data having a second logic value contrary to the first logical value if the fetched parity data is different from the input parity; and

a selecting unit for selecting the bank control data or the discrimination data in response to the bank information signals to generate the output data, wherein the selecting unit includes a plurality of multiplexers for providing one of the discrimination data and the bank control data as the output data in response to the bank information signals, and

wherein the refresh operation is independently performed with respect to the respective memory banks, and is prevented from being simultaneously performed with respect to two or more memory banks.

16. (Previously Presented) The SRAM-compatible memory according to claim 15, wherein the parity bank has a substantially same capacity and structure as each of the memory banks.

17. (Original) The SRAM-compatible memory according to claim 15, wherein the memory banks each independently store corresponding one of the input data.

18. (Original) The SRAM-compatible memory according to claim 15, wherein each of the memory banks independently performs a read-access operation in response to a read command externally provided.

19. (Cancelled)

20. (Cancelled)